Table of Contents: Volume 1 (1989)

Number 1

Editorial ..... *Earl E. Swartzlander, Jr.* 5

Introduction ..... *Jose A.B. Fortes and S.Y. Kung* 7

Bit-Level Systolic Architectures for High Performance IIR Filtering ..... *S.C. Knowles, R.F. Woods, J.G. McWhirter and J.V. McCanny* 9

Parallel Video Signal Processor Configuration Based on Overlap-Save Technique and its LSI Processor Element: VISP ..... *Takao Nishitani, Ichiro Tamitani, Hidenobu Harasaki, Yukio Endo, Toshiyki Kanou and Koichi Kikuchi* 25

A Million Transistor Systolic Array Graphics Engine ..... *Nader Gharachorloo, Satish Gupta, Erdem Hokenek, Peruvemba Balasubramanian, William Bogholtz, Christian Mathieu and Christos Zoulas* 35

Parallel Implementation of Synthetic Aperture Radar Algorithms ..... *K. Wojtek Przytula and J. Greg Nash* 45

Cellular Array Processor CAP and Applications ..... *Mitsuo Ishii, Hiroyuki Sato, Morio Ikesaka, Kouichi Murakami and Hiroaki Ishihata* 57

ASP Modules: Cost-Effective Building-Blocks for Real-time DSP Systems ..... *R.M. Lea* 69

Number 2

Editorial ..... *Earl E. Swartzlander, Jr.* 91

Introduction ..... *Jose A.B. Fortes and S.Y. Kung* 93

The Mapping of Linear Recurrence Equations on Regular Arrays ..... *Patrice Quinton and Vincent Van Dongen* 95

Scheduling a System of Nonsingular Affine Recurrence Equations onto a Processor Array ..... *Yoav Yaacoby and Peter R. Cappello* 115

Subspace Scheduling and Parallel Implementation of Non-Systolic Regular Iterative Algorithms ..... *V.P. Roychowdhury and T. Kailath* 127

A Systolic Algorithm and Architecture for Solving Sets of Linear Equations with Multi-Band Coefficient Matrix ..... *Paul F.C. Krekel and Ed F. Deprettere* 143

A Block Algorithm and Optimal Fixed-Size Systolic Array Processor ..... *Fernando J. Núñez and Mateo Valero* 153

Number 3

Editorial ..... *Earl E. Swartzlander, Jr.* 167

Fast Radix-2 Division with Quotient-Digit Prediction ..... *Milos D. Ercegovac and Tomas Lang* 169

A Novel Fault Tolerance Technique for Recursive Least Squares Minimization ..... *Franklin T. Luk, Erik K. Torng, Cynthia J. Anfinson* 181

An Efficient Bit-Level Systolic Cell Design for Finite Ring Digital Signal Processing Applications ..... *G.A. Jullien. P.D. Bird, J.T. Carr, M. Taheri, W.C. Miller* 189

On the Optimality of Linear Schedules ..... *Weijia Shang and Jose A.B. Fortes* 209

Parallel Algorithms/Architectures for Neural Networks ..... *J.N. Hwang and S.Y. Kung* 221

Number 4

Editorial ..... *Earl E. Swartzlander, Jr.* 255

A VLSI Structure for $X(\text{mod } m)$ Operation ..... *Giuseppe Alia and Enrico Martinelli* 257

An Integrated Automatic Design System for Complex DSP Algorithms ..... *J. v. Meerbergen, J. Huisken, P. Lippens, O. McArdle, R. Segers, G. Goossens, J. Vanhoof, D. Lanneer, F. Catthoor and H. De Man* 265

Bidiagonalization and Symmetric Tridiagonalization by Systolic Arrays ..... *Robert Schreiber* 279

Efficient Microcoded Processor Design for Fixed Rate DFT and FFT ..... *Francky Catthoor, Dirk Lanneer and Hugo De Man* 287

Systolic Algorithms for Some Scheduling and Graph Problems ..... *Oscar H. Ibarra, Tao Jiang, Jik H. Chang and Michael A. Palis* 307

A Case for Digit Serial VLSI Signal Processors ..... *Mary Jane Irwin and Robert Michael Owens* 321

Mapping Dynamic Programming onto a Linear Systolic Array ..... *V.K. Prasanna Kumar and Yu-Chen Tsai* 335

A Clock-Free Chip Set for High-Sampling Rate Adaptive Filters ..... *Teresa H.-Y. Meng, Robert W. Brodersen and David G. Messerschmitt* 345

Scalable VLSI Implementations for Neural Networks ..... *David Van den Bout, Paul Franzon, John Paulos, Thomas Miller III, Wesley Snyder, Troy Nagle and Wentai Liu* 367